You may discuss with other students, but all programs and the requested diagram should be your own work. Include the Stevens honor pledge either in your submission itself or as a comment on your submission.

Suppose you are asked to create a FSM that can detect a sequence that meets the following qualifications:

* The machine is looking for a sequence of 5 consecutive bits
* The sequence should involve exactly one “flip”
  + A “flip” in the sequence involves switching from 0 to 1 or from 1 to 0. I intentionally do not list examples so that not everyone does the exact same sequence, but feel free to check with me if you are not sure.

For either a Mealy OR a Moore machine, create a diagram for the FSM that could detect your chosen sequence, then implement the design in VHDL.

Example code for a different sequence as well as a testbench implementation are provided in our Github repository here (designFSM and testbenchFSM): <https://github.com/byett/dsd/tree/CPE487-Fall2024/ghdl>.

You can modify these to replicate the behavior of the FSM you designed, or if you prefer a different programming approach you may start from scratch.

You should submit the code, including evidence that the code worked via an appropriate testbench implementation that successfully triggers the output of the FSM at least one time. Also submit a picture of your drawn diagram, which can be done via hand drawings or virtual drawings.